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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,490	12/22/2000	George Beshara Bendak	AMCC4820	8935

7590 01/11/2005

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EXAMINER	
SHEW, JOHN	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/746,490	BENDAK ET AL.
	Examiner	Art Unit
	John L Shew	2664

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 60 is/are allowed.

6)☒ Claim(s) 1,13-15,17-22,24,26-28,30,33,38 and 48 is/are rejected.

7)☒ Claim(s) 2-12,16,23,25,29,31-32,34-37,39-47,49-59 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12222000.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Page 11 line 17 cites "filed _____" should be replaced with the corresponding application number and date.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 13, 17, 18, 19, 20, 21, 22, 24, 30, 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Bellisio.

Claim 1, Bellisio teaches a method of transmission of a multidimensional digital frame structure (Abstract lines 1-5) referenced by the digital transmission of interleaved tributary signals, for varying the location of frame synchronization bytes (Abstract lines 5-7, FIG. 3) referenced by the sliding auxiliary frame pattern F_T, the method comprising defining a frame with an overhead section having a predetermined number of bytes (FIG. 3) referenced by the frame with sections composed of auxiliary frame pattern F_T Data and overhead section OH, and selecting the location of the bytes in the overhead section to be used for frame synchronization (FIG. 3, column 1 lines 40-47, column 2 lines 20-30) referenced by preprocessor shifting of the auxiliary frame pattern F_T relative to its data stream.

Claim 13, Bellisio teaches a method for the receiving of a multidimensional digital frame structure (Abstract lines 1-5, FIG. 6, column 30 lines 30-36) referenced by the receiver demultiplexer 169 receiving multidimensional interleaved frames, for varying the location of frame synchronization bytes (Abstract lines 5-7, FIG. 3) referenced by the sliding auxiliary frame pattern F_T, the method comprising defining a frame with an overhead section having a predetermined number of bytes (FIG. 3) referenced by the frame with sections composed of auxiliary frame pattern F_T Data and overhead section OH, and selecting the location of the bytes in the overhead section to be used for frame synchronization, (FIG. 3, column 1 lines 40-47, column 2 lines 20-30) referenced by preprocessor shifting of the auxiliary frame pattern F_T relative to its data stream.

Claim 17, Bellisio teaches selecting the number of bytes in the overhead section to be used for frame synchronization (FIG. 3, column 2 lines 20-36) referenced by the selecting the one F_T byte associated to the F_T / Data / OH section.

Claim 18, Bellisio teaches selecting the value of the frame synchronization bytes (FIG. 3, column 2 lines 20-39) referenced by selection of the F_T pattern value from the F_S pattern value for detection.

Claim 19, Bellisio teaches a method for varying the location of frame synchronization bytes in the communication of a multidimensional digital frame structure (Abstract lines 1-7, FIG.3) referenced by the digital transmission of interleaved tributary signals which are multidimensional with a sliding auxiliary frame pattern F_T, the method comprising selecting the location of frame synchronization bytes in the overhead section of a transmitted frame (FIG. 3, column 1 lines 40-47, column 2 lines 20-30) referenced by overhead section of F_T/Data/OH with a preprocessor shifting of the auxiliary frame pattern F_T relative to its data stream requiring selection of the location, sending the frame (FIG. 6) referenced by MUX 157 sending the frame, receiving the frame (FIG. 6) referenced by MUX 167 receiving the frame, and synchronizing the received frame in response to recognizing the frame synchronization bytes (FIG. 6, FIG. 7, column 8 lines 30-32) referenced by the de-interleaver 167 and associated framing decoding circuitry.

Claim 20, Bellisio teaches selecting the number of consecutive frames that must be recognized (FIG. 7, column 9 lines 11-23) referenced by the overhead process circuitry 172 to determine the number of pulses required to achieve framing from the Frame On F_{TO} circuit 175, and wherein synchronizing the received frame in response to recognizing the frame synchronization bytes includes synchronizing the received frame in response to the selected number of recognized frames (FIG. 7, column 8 lines 48-64) referenced by the framing circuit 175 arranged to frame on the F_{TO} byte with reading of the associated overhead for the proper byte.

Claim 21, Bellisio teaches selecting the location of the bytes to be used for the frame synchronization of received frames (FIG. 3, column 1 lines 40-47, column 2 lines 20-30, FIG. 6) referenced by overhead section of F_T/Data/OH with a preprocessor shifting of the auxiliary frame pattern F_T relative to its data stream requiring selection of the location by the receiving demultiplexer 167, and wherein synchronizing the received frames includes recognizing frame synchronization bytes in response to the selected locations of the frame synchronization bytes in the received frame (FIG. 7, column 8 lines 48-64) referenced by the framing circuit 175 arranged to frame on the F_{TO} byte with reading of the associated overhead for the proper byte.

Claim 22, Bellisio teaches wherein selecting the location of the frame synchronization bytes in the received frame includes selecting first locations (FIG. 6, FIG. 7, column 8 lines 48-59) referenced by the Frame on F_{TO} circuit 175 selecting to frame on the F_{TO}

byte from preprocessor 159, and wherein synchronizing the received frame in response to recognizing the frame synchronization bytes includes synchronizing the received frame in response to recognizing frame synchronization bytes in the first locations (FIG. 6, FIG. 7, column 8 lines 48-61) referenced by the demultiplexer 169 receiving the frame and selecting the F_{TO} byte based on reading the associated overhead for the proper byte.

Claim 24, Bellisio teaches selecting the location of frame synchronization bytes in the overhead section of a transmitted frame (FIG. 3, column 1 lines 40-47, column 2 lines 20-30, FIG. 6) referenced by overhead section of F_T/Data/OH with a preprocessor shifting of the auxiliary frame pattern F_T relative to its data stream requiring selection of the location by the receiving demultiplexer 167, includes selecting a first number of frame synchronization byte locations (FIG. 6, FIG. 7, column 8 lines 41-59) referenced by the selection of the first F_{TO} byte which is determined by reading the associated overhead for the proper byte, and wherein selecting the location of the bytes to be used for frame synchronization of the received frame includes selecting locations for the first number of frame synchronization bytes (FIG. 6, FIG. 7, column 8 lines 41-59) referenced by the selection of the selection of one of three F_{TO} signals on the demultiplexer output of line a1.

Claim 30, Bellisio teaches selecting the number of frame synchronization bytes required for the recognition of a received frame (FIG. 7, column 9 lines 11-23) referenced by the

overhead process circuitry 172 to determine the number of pulses required to achieve framing from the Frame On F_{TO} circuit 175.

Claim 33, Bellisio teaches selecting the value of the frame synchronization byte in each byte location (FIG. 3, column 2 lines 20-39) referenced by selection of the F_T pattern value from the F_S pattern value for detection at byte location identified by delay offset τ_o.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14, 15, 26, 27, 28, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bellisio as applied to claims 1, 13, 17, 18, 19, 20, 21, 22, 24, 30, 33 above, in view of Sands.

Claims 14, 15, Bellisio teaches a slidable auxiliary frame pattern used in multilevel multiplexing. Bellisio does not teach selecting a bit error rate for frame synchronization. Sands teaches selecting a bit error rate required for the recognition of a frame synchronization byte (column 1 lines 30-34, column 3 lines 9-17, column 3 lines 54-56)

referenced by the pattern detection circuitry allowing for a programmable prescribed bit error rate wherein the pattern detected is the framing pattern.

Sands teaches selecting a frame synchronization byte bit error rate includes selecting an average bit error rate for the frame synchronization bytes in the selected location (column 3 lines 49-56) referenced by the acceptable bit error rate being programmable which is an average of the bit error for it must be determined over a time period and the frame sync byte is the programmable pattern to be detected.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the prescribed bit error rate of Sands to the detection of the auxiliary frame pattern of Bellisio for the purpose of satisfying a prescribed criterion before declaring that the pattern has been successfully acquired.

Claims 26, 27, 28, Bellisio teaches a slidable auxiliary frame pattern used in multilevel multiplexing. Bellisio does not teach selecting a bit error rate for frame synchronization. Sands teaches selecting the bit error rate required for the recognition of a frame synchronization byte in a received frame (FIG. 1A, column 1 lines 30-34, column 3 lines 9-17, column 3 lines 54-56) referenced by the pattern detection circuitry allowing for a programmable prescribed bit error rate wherein the pattern detected is the framing pattern on the received serial data stream TDATA 27.

Sands teaches selecting a bit error rate includes selecting an average bit error rate for the frame synchronization bytes in the selected locations (column 3 lines 49-56) referenced by the acceptable bit error rate being programmable which is an average of

the bit error for it must be determined over a time period and the frame sync byte is the programmable pattern to be detected.

Sands teaches synchronizing the received frame in response to recognizing the frame synchronization bytes includes recognizing frame synchronization bytes having a bit error rate less than or equal to the selected frame synchronization bit error rate (column 7 lines 51-67, column 8 lines 1-3) referenced by the BER used to calculate the REG digital code value for maximum pattern match used by the comparator for synchronization.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the prescribed bit error rate of Sands to the detection of the auxiliary frame pattern of Bellisio for the purpose of satisfying a prescribed criterion before declaring that the pattern has been successfully acquired.

Claims 38, 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bellisio as applied to claims 1, 13, 17, 18, 19, 20, 21, 22, 24, 30, 33 above, in view of Birch et al.

Claim 38, Bellisio teaches a multidimensional digital frame structure (Abstract lines 1-5) referenced by the digital transmission of interleaved tributary signals, a transmitter

system for varying the location of frame synchronization bytes (FIG. 6, Abstract lines 5-7) referenced by the frame with sliding auxiliary frame pattern F_T output by transmitter MUX 157, the system comprising a frame generator including an overhead generator to generate the overhead section of a frame (FIG. 3, FIG. 4, column 6 lines 34-38) referenced by Overhead Process circuit 105 to generate the overhead section, a payload generator to generate the payload section of the frame (FIG. 4, column 6 lines 11-22) referenced by the Pseudo Random Word Descramble circuit 75 in conjunction with the 2 Byte Shift Register 77 handling of interleave data, wherein the overhead generator includes an input to select the location of frame synchronization bytes in the overhead section (FIG. 4, column 7 lines 12-20) referenced by the New F_{TO} Byte + OH circuit 93 which selects the appropriate location of the outgoing F_{TO} byte and overhead bits. Bellisio does not teach Forward Error Correction.

Birch teaches an encoder to provide forward error correction (FEC) for the frame (FIG. 2B, FIG. 4, column 13 lines 29-34) referenced by the Reed Solomon Forward Error Correction unit 454.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the FEC unit of Birch to the multilevel multiplex transmission system of Bellisio for the purpose of transmission of a plurality of services over limited bandwidth and in noisy error-prone environments.

Claim 48, Bellisio teaches a multidimensional digital frame structure (Abstract lines 1-5) referenced by the digital transmission of interleaved tributary signals, a receiver system for varying the location of frame synchronization bytes (FIG. 6, Abstract lines 5-7) referenced by the frame with sliding auxiliary frame pattern F_T received by demultiplexer MUX 167, the system comprising a frame receiver including an overhead receiver to receive the overhead section of a frame (FIG. 7, column 9 lines 11-23) referenced by Overhead Process circuit 172, a payload receiver to receive the payload section of the frame (FIG. 7, column 9 lines 43-52) referenced by the DeScrambler 191 to output data line a_1 , and wherein the overhead receiver includes an input to select the location of frame synchronization bytes in the overhead section to be used for frame synchronization (FIG. 7) referenced by the Frame on F_{TO} circuit 175 sending select output to the Overhead Process 172 via the DL τ_{OH} circuit 179 as to the location of the sync byte. Bellisio does not teach Forward Error Correction.

Birch teaches a decoder to provide forward error correction (FEC) for the frame (FIG. 2B, FIG. 5, column 13 lines 58-62) referenced by the Reed Solomon Forward Error Correction decoder unit 588.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the FEC unit of Birch to the multilevel multiplex transmission system of Bellisio for the purpose of transmission of a plurality of services over limited bandwidth and in noisy error-prone environments.

Allowable Subject Matter

4. Claims 2-12, 23, 25, 29, 31, 32, 34, 35, 36, 37, 39, 40, 41, 42, 43, 44, 45, 46, 47, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 60 is allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art search did not disclose a frame synchronization method inclusive of generator/receiver able to accept commands to select the location and values of synchronization bytes within a frame.

Citation of Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Patent number 5400369, Ikemura disloses a frame aligner with reduced circuit scale. Patent number 6400734, Weigand discloses a method for TDMA receiver incorporating a unique word correlation control loop. Patent number 6445719, Schneider et al. discloses a method for reducing synchronization and resynchronization times for systems with pulse stuffing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John L Shew whose telephone number is 571-272-3137. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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